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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,752	11/17/2003	Chun Chen	400.235US01	3378

27073 7590 04/12/2006

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EXAMINER	
PHAM, THANHHA S	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 04/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/714,752	CHEN ET AL.
	Examiner	Art Unit
	Thanhha Pham	2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 8-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 8-17* is/are rejected.

7)☒ Claim(s) *3* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to Applicant's Amendment dated 01/31/2006.

Specification

1. **The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter.** See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: Specification should be corrected to support limitations of original claim 3 of "wherein patterning the first and the second mask layers with the same pattern"

Drawings

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the exposed of source portion through the dielectric 275 of figure 2C (see specification [0043] for details) must be shown or the feature(s) canceled from the claim(s). In addition, the first mask (280) exposing a portion of the layer of dielectric over the drain region and the second mask (281) exposing a portion of the layer of polysilicon over the drain region as in claim 17 be shown or the feature(s) canceled from the claim(s).

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate

prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

3. Claims 2 and 15 objected to because of informalities. Appropriate corrections are required to clarify scopes of claims.

► With respect to claim 2, "wherein forming a first and second mask layer further comprises forming at least one of the first and second mask layer with a photoresist" should be changed to "wherein forming the first and second mask layers further comprises forming at least one of the first and second mask layers with a photoresist" to clarify scope of claim.

► With respect to claim 15, "wherein removing the first and second mask layer further comprises stripping at least one of the first and second mask layer" should be

changed to "wherein removing the first and second mask layers further comprises stripping at least one of the first and second mask layers" to clarify scope of claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-2, 4-6 and 8-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim [US 6,001,685] in view of Wu et al. [US 6,309,975] and Applicant's Admitted Prior Art.

► With respect to claims 1, 5-8 and 14, Kim (figs 6's and col. 1-7) discloses a method of fabricating a source interconnect to a memory cell comprising:

forming a layer of dielectric material (28/29/30, fig 6B) overlying a gate stack (23/24/25), a source region (26) and a drain region (28) of the memory cell;

forming a first mask layer (31, fig 6B) overlying the layer of dielectric material;

patterning the first mask layer (31, fig 6B) to expose a portion of the layer of dielectric material over at least the source region;

removing a portion of the exposed portion of the layer of dielectric material to expose the source region (26, fig 6C);

removing the first mask layer (31, fig 6C);

forming a layer of polysilicon (32, fig 6C) overlying the layer of dielectric material and in contact with the exposed source region; and

selectively etching the layer of polysilicon thereby forming the source interconnect (32', fig 6D).

Kim does not teach:

a) removing said portion of the exposed portion of the layer of the dielectric material to form a trench shaped region and expose the source region ***[claim 1];***

b) said selectively etching the layer of polysilicon comprising: forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the source region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect ***[claim 1]***, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon ***[claim 14]***, wherein said selectively etching the layer of polysilicon comprises selectively wet etching the layer of polysilicon ***[claim 5]*** with TMAH ***[claim 6]*** or KOH ***[claim 8].***

Regarding to **a)**, APA (fig 1B, specification paragraph [0023]) shows etching dielectric material can expose the source region and form in either a trench shaped

region or a contact hole shaped region to interconnection. Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Kim et al by forming the trench shaped region as being claimed as taught by APA to provide interconnection region to the source region of device.

Regarding to **b)**, Wu et al (figs 21-23, col. 8-11, 34-40 and 47-48) teaches forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over an active region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the polysilicon interconnect, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon, wherein said selectively etching the layer of polysilicon comprises selectively wet etching the layer of polysilicon with TMAH or KOH. Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Kim by using the second mask, implanting ions and selectively etch as being claimed, per taught by Wu et al., to provide a better control in selectively etching the layer of polysilicon to form the source interconnection.

► With respect to claim 2, Kim (col. 6 lines 16-30) disclose forming the first mask (first mask 31) with a photoresist.

► With respect to claim 4, the layer of polysilicon overlying the dielectric material and in contact with the exposed source region in the process of Kim in view of Wu et al and APA would be conductively doped for functioning as conductor polysilicon for the source interconnection.

► With respect to claim 9, the layer of polysilicon overlying the layer of dielectric material would be a layer of silicon containing layer.

► With respect to claims 12-13, the claimed range of ion dosage level of implanting ion is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

> "Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."
>
> *See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66*

USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

► With respect to claim 15, removing the first and second masks in the process of Kim in view of Wu et al and APA would comprise stripping the first and second masks.

► With respect to claim 16, Kim (col. 6 lines 26-35) discloses removing a portion of the exposed portion of the layer of dielectric material to expose the source region comprises anisotropically etching the exposed portion of the layer of dielectric material.

► With respect to claim 17, Kim (fig 6B-C) shows patterning the first mask layer comprising patterning the first mask layer to additionally expose a portion of the layer of dielectric over at least the drain region (26').

5. Claims 1-2, 4-6 and 8-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jenq et al. [US 6,159,788] in view of Wu et al [US 6,309,975] and APA.

► With respect to claims 1, 5-8 and 14, Jenq et al (figs 1-5 and col. 1-10) discloses a method of fabricating a source interconnect to a memory cell comprising:

forming a layer of dielectric material (36, fig 2) overlying a gate stack (14/16/18/20), a source region (30) and a drain region (28) of the memory cell;

forming a first mask layer overlying the layer of dielectric material (col. 6 lines 1-7);

patterning the first mask layer (having the first mask pattern with an opening over the source region 30, col. 6 lines 1-7) to expose a portion of the layer of dielectric material over at least the source region;

removing a portion of the exposed portion of the layer of dielectric material to expose the source region (fig 3, col. 6 lines 1-16);

removing the first mask layer (col 6 lines 28-29);

forming a layer of polysilicon (42, fig. 4) overlying the layer of dielectric material and in contact with the exposed source region; and

selectively etching the layer of polysilicon thereby forming the source interconnect (44, fig 5).

Kim does not teach:

a) removing said portion of the exposed portion of the layer of the dielectric material to form a trench shaped region and expose the source region ***[claim 1];***

b) said selectively etching the layer of polysilicon comprising: forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the source region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect ***[claim 1]***, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon ***[claim 14]***, wherein said selectively

etching the layer of polysilicon comprises selectively wet etching the layer of polysilicon ***[claim 5]*** with TMAH ***[claim 6]*** or KOH ***[claim 8].***

Regarding to **a)**, APA (fig 1B, specification paragraph [0023]) shows etching dielectric material can expose the source region and form in either a trench shaped region or a contact hole shaped region to interconnection. Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Jeng et al by forming the trench shaped region as being claimed as taught by APA to provide interconnection region to the source region of device.

Regarding to **b)**, Wu et al (figs 21-23, col. 8-11, 34-40 and 47-48) teaches forming a second mask layer overlying the layer of polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over an active region; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the polysilicon interconnect, wherein said implanting ion comprises implanting an ion species that is one of boron, phosphorous, arsenic, argon and silicon, wherein said selectively etching the layer of polysilicon comprises selectively wet etching the layer of polysilicon with TMAH or KOH. Therefore, at the time of invention, it would have been obvious for those skilled in the art to modify process of Jenq et al in view of APA by using the second mask, implanting ions and selectively etch as being claimed, per

taught by Wu et al., to provide a better control in selectively etching the layer of polysilicon to form the source interconnection.

► With respect to claim 2, Jenq et al (col. 6 lines 27-29) disclose forming at least one of the first and second masks (first mask) with a photoresist.

► With respect to claim 4, Jenq et al (col. 6 lines 30-45) discloses forming the layer of polysilicon overlying the layer of the dielectric material and in contact with the exposed source region wherein the layer of polysilicon is conductively doped.

► With respect to claim 9, the layer of polysilicon overlying the layer of dielectric material would be a layer of silicon containing layer.

► With respect to claim 10, Jenq et al (figs 2-3 and col 6 lines 1-7) disclose patterning the first mask layer comprises patterning the first mask layer to expose a portion of the layer of the dielectric over the source region and a portion of the gate stack.

► With respect to claim 11, in combination of process of Jenq et al in view of Wu et al and APA, to form the source interconnect (44) overlying the source region (30) and a portion of the gate stack, patterning the second mask would expose a portion of the layer of polysilicon over the source region and a portion of the gate stack.

► With respect to claims 12-13, the claimed range of ion dosage level of implanting ion is considered to involve routine optimization while has been held to be within the level of ordinary skill in the art. As noted in In re Aller 105 USPQ233, 255 (CCPA 1955), the selection of reaction parameters such as temperature and concentration would have been obvious.

"Normally, it is to be expected that a change in temperature, or in concentration, or in both, would be an unpatentable modification. Under some circumstances, however, changes such as these may be impart patentability to a process if the particular ranges claimed produce a new and unexpected result which is different in kind and not merely degree from the results of the prior art...such ranges are termed "critical ranges and the applicant has the burden of proving such criticality... More particularly, where the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation."

See also In re Waite 77 USPQ 586 (CCPA 1948); In re Scherl 70 USPQ 204 (CCPA 1946); In re Irmscher 66 USPQ 314 (CCPA 1945); In re Norman 66 USPQ 308 (CCPA 1945); In re Swenson 56 USPQ 372 (CCPA 1942); In re Sola 25 USPQ 433 (CCPA 1935); In re Dreyfus 24 USPQ 52 (CCPA 1934).

► With respect to claim 15, removing the first and second masks in the process of Jenq et al in view of Wu et al and APA would comprise stripping the first and second masks.

Response to Arguments

6. Applicant's arguments filed on 01/31/2006 have been fully considered but they are not persuasive.

► In regarding to Applicant's argument on pages 9-11, Applicant argues that claims 1-2, 4-6 and 8-17 are not obvious over Kim [US 6,001,685] in view of Wu et al [US 6,309,975] and Applicant's Admitted Prior Art because:

- Kim does not disclose or suggest forming a local interconnect by forming a trench shaped region in a dielectric layer then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted region of a deposited layer polysilicon;
- Wu et al does not has found no mention of forming a trench shape local interconnect by forming a trench shape region in a dielectric layer, depositing a layer of polysilicon, masking the layer of polysilicon, selectively ion implanting the masked layer of polysilicon so that it can selectively etched to preferentially remove the non-implanted portion thereby forming a source interconnect in the trench shape region; and
- APA does not teach or suggest Applicant method of forming a trench shaped local interconnect, second mask layer, ion implant and wet etch -- APA (fig 1B text [0023]) does not teach or suggest forming a local interconnect of polysillicon by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon.

The argument is not persuasive since Applicant can not attack references individually while the rejection is based on a combination of obviousness. The test for

obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this situation, Kim substantially discloses the claimed method including forming the source interconnect (32', fig 6D) in the layer of the dielectric and being in contact with the exposed source region. Although Kim does not mention about said local interconnect in the trench shaped region in the dielectric material exposing the source region, such as teaching is suggest by APA (fig 1B, lines 5-9 of text [0023]). In addition, Wu et al teaches patterning the second mask to expose a portion of the layer of polysilicon, selectively ion implanting the masked layer of polysilicon so that it can selectively etched to preferentially remove the non-implanted portion thereby interconnect of polysilicon. Combination of process of Kim in view of APA and Wu et al would suggest the claims with reason given above to form the source interconnect in the trench shaped region.

► In regarding to Applicant's argument on pages 11-14, Applicant argues that claims 1-2, 4-6 and 8-17 are not obvious over Jenq et al [US 6,159,788] in view of Wu et al [US 6,309,975] and Applicant's Admitted Prior Art because:

- Jenq et al teach forming an electrode for DRAM storage capacitor but does not teach forming a local interconnect by forming a trench shaped

region and by selectively etching non-ion implanted region of a deposited layer of polysilicon;

- Wu et al does not teach forming a trench shape local interconnect by forming a trench shaped region in a dielectric layer, depositing a layer of polysilicon, masking, selectively ion implanting then selectively etching to preferentially remove the non-implanted portion thereby forming the source interconnect in the trench shape region; and
- APA (fig 1B text [0023]) does not teach or suggest Applicant method of forming a trench shaped local interconnect, second mask layer, ion implant and wet etch -- APA does not teach or suggest forming a local interconnect of polysillicon by forming a trench shaped region in a dielectric layer and then forming a local interconnect of polysilicon in the trench shaped region by selectively etching non-ion implanted regions of a deposited layer of polysilicon.

The argument is not persuasive since Applicant attacks references individually while the rejection is based on a combination of obviousness. The test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this situation, contrary to Applicant argument, Jenq et al substantially discloses the claimed method of forming

local interconnect (polysilicon pad 44, fig 5) of polysilicon over which a electrode (54, fig 10) of DRAM storage capacitor will be formed. Although Jenq et al not mention in written that the local interconnect is formed in the trench shaped region in the dielectric, such as teaching is taught by APA (fig 1B, lines 5-9 of text [0023]). Moreover, Wu et al teaches selectively ion implanting the masked layer of polysilicon so that it can selectively etched to preferentially remove the non-implanted portion thereby interconnect of polysilicon. Therefore, combination of process of Jenq et al in view of APA and Wu et al would suggest the claims with reason given above to form the source interconnect in the trench shaped region.

Allowable Subject Matter

7. Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Recording Prior Art fails to disclose or suggest a combination process steps of fabricating a source interconnect to a memory cell comprising patterning the first mask layer to expose a portion of the layer of dielectric material over at least the source region; removing a portion of the exposed of the layer of dielectric material to form a trench shaped region and expose the source region; forming a layer of polysilicon overlying the layer of dielectric material and trench shaped region to be in contact with the exposed source region; forming a second mask layer overlying the layer of

polysilicon; patterning the second mask layer to expose a portion of the layer of polysilicon over at least the trench shaped region; wherein patterning the first and second mask layers comprises patterning the first and second mask layers with the same pattern; implanting ions in the exposed portion of the layer of polysilicon, thereby forming an implanted portion of the layer of polysilicon and an non-implanted portion of the layer of polysilicon; removing the second mask layer; and selectively etching the layer of polysilicon to preferentially remove the non-implanted portion, thereby forming the source interconnect in the trench shaped region.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

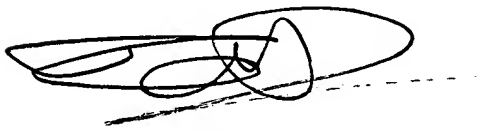
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanhha Pham whose telephone number is (571) 272-

1696. The examiner can normally be reached on Monday and Thursday 9:00AM - 9:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thanhha Pham
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